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09/703,034	10/31/2000	Joseph R. Zbiciak	TI-30553	8913

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/703,034	ZBICIAK, JOSEPH R.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13 and 25-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13 and 25-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 04/09/2007.

2. Claims 13 and 25-29 are pending in this application. Claims 13 and 25 are independent claims. In Amendment, claims 1-12 and 14-24 are cancelled and claims 25-29 are newly added. This Office Action is made final.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 28, the limitations "said first Q shifter...specified number of bits" in lines 6-7 and "said second Q shifter shifting...specified number of bits" in lines 10-12 are unclear since these limitations are incomplete. For examination purposes, the examiner considers the first limitation as "said first Q shifter shifting said first product by specified number of bits in response to the instruction" and the second limitation as "said second Q shifter shifting said second product by specified number of bits in response to the instruction".

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 13 and 25-29 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 13 and 25-29 cite a system and apparatus for performing a dot product in accordance with a mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result. However, claims 13 and 25-29 merely disclose steps/components for performing a dot product without further disclosing a practical/physical application or a useful and tangible result since the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein. Therefore, claims 13 and 25-29 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saishi et al. (U.S. 6,167,419) in view of Pitsianis et al. (U.S. Patent Application Publication No. 2003/00088601).

Re claim 13, Saishi et al. disclose in Figures 5-9 a digital system having a microprocessor (e.g. col. 1 lines 5-10 for processing digital signals) operable to execute a rounding product instruction (e.g. abstract and Figure 5 wherein the product is output of multiplication 505 and the rounding is done by rounding signal 514), wherein the microprocessor comprises: storage circuitry for holding pairs of elements (e.g. Figure 5 and Figure 8 wherein storage is used to hold the multiplier and multiplicand for input into the multiplication means 503); a multiply circuit (e.g. multiplication means 503 in Figure 5, in particular the multiplier for generating subproducts 505) connected to receive a first number of pairs of elements from the storage circuitry in a first execution phase of the microprocessor responsive to the product instruction (e.g. the multiplication means 503 is used to multiply the multiplier and multiplicand as pairs of elements together in Figure 5), the multiply circuit (e.g. multiplication means 503 in Figure 5 or Figure 8 for generating multiplication result 803) comprising a plurality of multipliers equal to the first number of pairs of elements (e.g. multiplication means in Figure 5 as single multiplication means corresponding to single pair of elements multiplier 501 and multiplicand 502 in Figure 5); an adder/subtractor circuit (e.g. an adder means including components 506-508 in Figure 5) having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers (e.g. inputs 505 as subproducts of multiplications between multiplier 501 and multiplicand 502

in Figure 5) and a mid-position carry (e.g. rounding signal 515 in Figure 5) input to a predetermined bit (e.g. predetermined bit is predetermined rounding position 805 in Figure 8 and col. 8 lines 15-17) for mid-position rounding (e.g. wherein the mid-position rounding is set when the rounding position is set at mth rounding position as seen in Figure 8) responsive to the rounding product instruction (e.g. abstract and Figure 5 wherein the product is output of multiplication 505 and the rounding is done by rounding signal 514 and component 512 in Figure 5); and a shifter (e.g. components 510 and 520 in Figure 5) connected to receive an output of the adder/subtractor circuit (e.g. multiplication with rounding signal added 509 in Figure 5), the shifter operable to shift a selected amount in response to the rounding product instructions (e.g. corresponding to instruction control means 512 in Figure 5).

Saishi et al. fail to disclose in Figures 5-9 product instruction is the dot product instruction for multiplying multiple pairs of elements. However, the dot product instruction for multiplying multiple pairs of elements is well known in the art of technology as addressed in Pitsianis et al.'s invention. Pitsianis et al. disclose in Figure 3B and 6 the dot product instruction for multiplying multiple pairs of elements wherein the dot product instruction is an instruction for performing complex multiplication as seen in Figures 3B and 9. In extension, the dot/complex product instruction for performing multiplication between multiple pars of elements is seen in Figures 3B or 6 wherein it discloses the fetching a first pair of elements (e.g. Xr and Yi in 603 and 605) and a second pair of elements (e.g. Xi and Yr in 603 and 605); forming a first product (e.g. result 617 as Xr*Yi) of the first pair of elements and a second product (e.g. result

619 as Xi*Yr) of the second pair of elements; combining (e.g. component 625 for adding) the first product with the second product; form a combined product as result (e.g. output of 625 as result of addition or output of 623 as result of subtraction of sub-products).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a dot product operation for multiplying multiple pars of elements as seen in Pitsianis et al.'s invention into Saishi et al.'s invention because it would enable to efficiently compute the sum of products inwhich would be used in many practical applications (e.g. FFT as seen in abstract and paragraphs [0002-0005] in column 1).

9. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saishi et al. (U.S. 6,167,419) in view of Peleg et al. (U.S. 6,385,634).

Re claim 25, Saishi et al. disclose in Figures 5 and 9 a data processing apparatus (e.g. Figure 5 and col. 1 lines 5-10 for processing digital signals in image and sound processing fields) comprising: a first multiply circuit (e.g. multiplication means 503 in Figure 5) having first and second inputs and an output (e.g. multiplier 501 and multiplicand 502 as inputs and subproducts 505 as output in Figure 5), said first multiply circuit operable in response to a product instruction to multiply data received at said first and second inputs (e.g. multiplier 501 and multiplicand 502) and generate a first product at said output (e.g. output of component 504 as subproducts 505 in Figure 5); an adder/subtractor circuit (e.g. components 506-508 as adder for adding inputs in Figure 5) having first and second inputs (e.g. output of component 504 as subproducts 505 in

Figure 5), a mid-position carry input (e.g. rounding signal 515 in Figure 5) to a predetermined bit (e.g. predetermined bit is predetermined rounding position 805 in Figure 8 and col. 8 lines 15-17) and an output (e.g. output of component 508 in Figure 5), said first input receiving said first product from said first multiply circuit (e.g. plurality of subproducts 505 in Figure 5), said adder/subtractor circuit (e.g. components 506-508 in Figure 5) operable in response to said product instruction to arithmetically combine said first and second products and a "1" input at said mid-position carry input of said predetermined bit thereby forming a mid-position rounded sum (e.g. the combination is performed at component 506 in Figure 5 and arithmetic representation is seen in Figure 8); and a shifter (e.g. components 510 and 520 in Figure 5) connected to receive an output of the adder/subtractor circuit (e.g. multiplication with rounding signal added 509 in Figure 5), the shifter operable to shift a selected amount in response to the rounding product instructions (e.g. corresponding to instruction control means 512 in Figure 5). Saishi et al. fail to disclose the dot product instruction having a second multiply circuit having first and second inputs and an output, said second multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a second product at said output; and an adder/subtract is receiving said first and second product from said first and second multiply circuits respectively. However, Peleg et al. discloses in Figures 1 and 8 the dot product instruction (e.g. packed instruction set 140 in Figure 1 and col. 17 line 49 to col. 19 line 33) having a second multiply circuit having first and second inputs and an output (e.g. multipliers 810-813 in Figure 8 wherein each of multiplier multiplies pair of corresponding elements to yield

corresponding product), said second multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a second product at said output (e.g. let say output of multiplier 810 as first product of first multiplier and multiplier 811 as second product of second multiplier in Figure 8); and an adder/subtract (e.g. component 850 in Figure 8) is receiving said first and second product from said first and second multiply circuits respectively (e.g. Figure 8). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the dot product instruction having a second multiply circuit having first and second inputs and an output, said second multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a second product at said output; and an adder/subtract is receiving said first and second product from said first and second multiply circuits respectively as seen in Peleg et al.'s invention into Saishi et al.'s invention because it would enable to efficiently compute the sum of products inwhich would be used in many practical applications (e.g. col. 17 lines 49-60 and col. 19 lines 25-33).

Re claim 26, Saishi et al. disclose arithmetic combination of subproducts is an arithmetic sum (e.g. component 506 in Figure 5). Saishi et al. fail to disclose the arithmetic combination of said first and second products. However, Peleg et al. disclose the arithmetic combination of said first and second products as sum (e.g. Figure 8). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the arithmetic combination of said first and second products as sum as seen in Peleg et al.'s invention into Saishi et al.'s invention because it

would enable to efficiently compute the sum of products inwhich would be used in many practical applications (e.g. col. 17 lines 49-60 and col. 19 lines 25-33).

Re claim 27, Saishi et al. fail to disclose dot product instruction is a dot product with negate instruction; and said arithmetic combination of said first and second products is a difference of said second product from said first product in response to said dot product with negate instruction. However, Peleg et al. disclose dot product instruction is a dot product with negate instruction (e.g. packed instruction set 140 in Figure 1); and said arithmetic combination of said first and second products is a difference of said second product from said first product in response to said dot product with negate instruction (e.g. Figure 8 with subtraction is set). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add dot product instruction is a dot product with negate instruction; and said arithmetic combination of said first and second products is a difference of said second product from said first product in response to said dot product with negate instruction as seen in Peleg et al.'s invention into Saishi et al.'s invention because it would enable to efficiently compute the sum of products inwhich would be used in many practical applications (e.g. col. 17 lines 49-60 and col. 19 lines 25-33).

Response to Arguments

10. Applicant's arguments filed 04/09/2007 have been fully considered but they are not persuasive.

a. The applicant argues in page 5 last paragraph for claims rejected under 35 U.S.C. 101 that the claims are statutory since claim is not a method claim. The claim is an apparatus claim having tangible parts as storage, multiplier, adder/subtractor, and shifter.

The examiner respectfully submits that the claims are still directed to non-statutory subject matter under current language. The claims only disclose the general circuit components for performing basic mathematical operations. The claims fail to cite any a practical/physical application, having arithmetic operations in circuit would appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein.

b. The applicant argues in pages 16-17 for claim 13 that the cited references by Saishi et al. and Pitsianis et al. fail to disclose an adder/subtractor circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products form a plurality of multipliers and a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction. In particular, neither the references fails to teach combining two products and rounding in a single adder/subtractor circuit as recited in claim 13.

The examiner respectfully submits that these argued features are either clearly, expressively, or inherently seen in combination of both references by Saishi et al. and Pitsianis et al. In general, the primary reference by Saishi et al. discloses a single set of operand multiplication with rounding processes as recited in the claim wherein the secondary reference is combined to disclose a plurality set of operands multiplication. Thus, the combination of references clearly disclose a plurality multiplication of sets of operands (e.g. more than one multiplication or product) and a single adder/subtractor circuit (e.g. adder circuit) is used to add all the products (e.g. produce by multipliers) with a rounding signal to yield a sum rounded of products as cited in the claims. The single adder/subtractor circuit of the claimed invention is the adder means 506-508 in the primary reference Figure 5 wherein this single adder means will sum all the outputs from multipliers (e.g. as subproducts and from secondary reference) along with a rounding signal 515 in Figure 5 at appropriated place for rounding at mid-position. Therefore, the primary reference discloses a combination of a single product and rounding in a single adder/subtractor circuit wherein the secondary reference discloses a combination of two products.

c. The applicant argues in pages 7-8 for claim 13 that the cited references fail to disclose a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction.

The examiner respectfully submits that the current language does not clearly address when (e.g. before the multiplication, during the multiplication, or after the multiplication) the predetermined bit is determined for adding or inserting a carry input bit. Thus as long as a carry bit is appropriately added to mid-position of result, it meets the limitations cited in the claim. Further, the position to add the carry bit in the primary reference is not randomly determined but rather it is either algorithm/desired determined/calculated right before the adding process. The paragraph in column 8 lines 27-40 with support of Figure 8 clearly indicated a mid-position rounding wherein the predetermined rounding position 811 (e.g. lines 29-30 in column 8) is located at the mth bit wherein the kth bit can be set at 0.

d. The applicant argues in pages 9-10 corresponding to the response to arguments of the last office action for claim 13 that primary reference fails to disclose to add two products as required in claim 13. Further, claim 13 clearly requires to have a single integrated adder is used to combine two product and round the result.

The examiner respectfully submits that the second product is expressively seen in the secondary reference as clearly addressed in the above rejection and argument wherein the primary reference only discloses a single product and an adder for adding the product with carry-bit inputs at desired place (e.g. mid-position as seen in Figure 8); the secondary reference discloses an adder for adding multiple products; it is obvious to combine both references in order to discloses every

single limitations cited in claim 13. Further as previously mentioned by the examiner, the "a single integrated adder" is seen in Figure 5 with components labels 506-508 for adding product 505 with carry-in bit 515.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

July 31, 2007